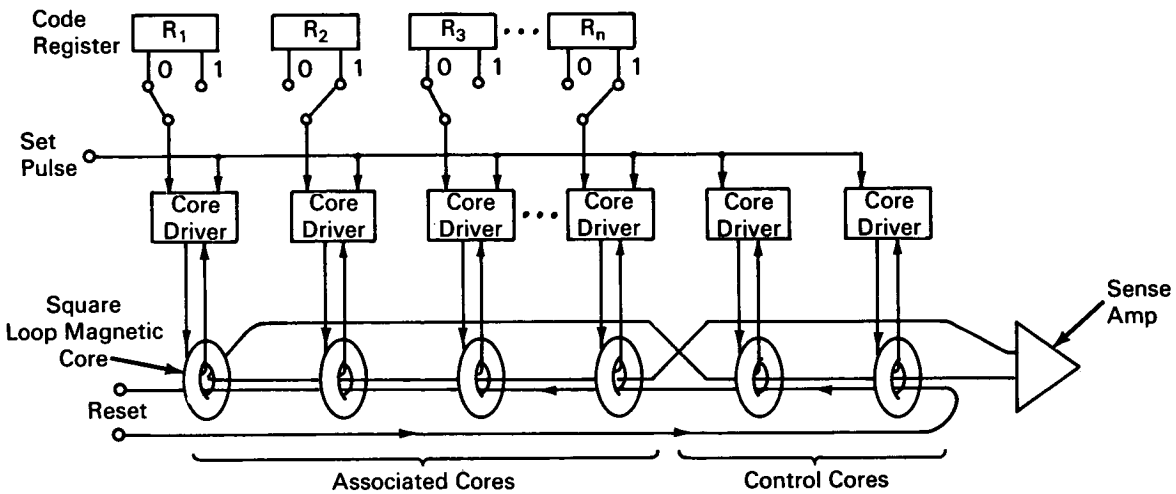
NASA TECH BRIEF

Digital System Detects Binary Code Patterns Containing Errors



The problem:

In pulse code modulation (PCM) systems, digital code patterns containing errors frequently result in loss of telemetry information. Prior methods of overcoming this deficiency, including conversion to analog voltage pulses and comparison to a reference, have been costly in equipment and time consuming.

The solution:

A system of square loop magnetic cores associated with code input registers to react to input code patterns by reference to a group of control cores in such a manner that errors are canceled and patterns containing errors are accepted for amplification and processing.

How it's done:

All cores are initially in the zero or "reset" state. The code to be compared with the desired code is stored in the register R_1 through R_N. Each register stage has an associated magnetic core and drive circuit. To test for the desired code, each core is "set" if the associated bit is *not* the desired bit. (Thus if the register contains the desired code, no cores would be "set".) In addition the control core or cores are also "set". All cores are now given a "reset" pulse, but only those cores that were "set" will induce a voltage on the sense wire. The sense winding is threaded through the register cores so that the induced voltage will be minus one unit for each core that was "reset". The sense winding is threaded through the control cores so that a voltage of plus one unit of voltage will be induced for each core threaded. The sense amplifier is adjusted to respond to voltages in excess of $+¾$ unit voltage. If only one control core is used, the sense voltage will exceed $+¾$ unit only if a perfect code is contained in the register. If one error

(continued overleaf)

is to be allowed, two control cores are used. In this way, one of the control cores will cancel the induced voltage from the error core and the second control core will cause the sense voltage to exceed $+\frac{3}{4}$ unit voltage. If a perfect code is in the register, both control cores will give $+2$ units of voltage to the sense amplifier which is more than enough to give an output from the sense amplifier.

Notes:

1. Any number of errors may be tolerated by this embodiment by simply adding additional control cores such that there is one more control core than the number of errors to be tolerated.
2. This technique should improve reception capabilities in PCM telemetry systems.
3. Inquiries concerning this innovation may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland 20771
   Reference: B66-10516

Patent status:

No patent action is contemplated by NASA.

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